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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

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|---|---|
| UNITED STATES OF AMERICA,<br><br>Plaintiff,<br><br>v.<br><br>FUJIAN JINHUA INTEGRATED CIRCUIT CO., LTD.<br><br>Defendant. | **CASE NO. 18-CR-465 MMC**<br><br>**UNITED STATES' BILL OF PARTICULARS**<br><br>Courtroom: 7, 19th Floor<br>Hearing Date: June 23, 2021<br>Hearing Time: 2:15 PM |

The United States hereby provides the following particulars regarding Trade Secrets 1-8, as alleged in the Indictment.

1. The United States will prove that Trade Secrets 1-8 meet the definition of "trade secret" in 18 U.S.C. § 1839(3) of "all forms and types of financial, business, scientific, technical, economic, or engineering information . . . whether tangible or intangible, and whether or how stored compiled, or memorialized, physically, electronically, graphically, photographically, or in writing," and that (1) Micron took reasonable measures to protect Trade Secrets 1-8 and (2) each of Trade Secrets 1-8 derives independent economic value, actual or potential, from not being generally known to, and not being readily ascertainable through proper means by, another person who can obtain economic value from the disclosure or use of the information.
2. To further show that the information in Trade Secrets 1-8 is a type of "financial, business, scientific, technical, economic, or engineering information," the United States will prove that the information in each of Trade Secrets 1-8 is the following type of information, specifically identified in § 1839(3), as examples of "financial, business, scientific, technical, economic, or engineering information": (1) plans, (2) compilations,[1] (3) designs, (4) methods, (5) techniques, (6) processes, and (7) procedures.
3. For Trade Secrets 2-8, the United States will argue that the information in each document (considered as a whole document) specified in the Indictment as composing each of Trade Secrets 2-8 is a trade secret under 18 U.S.C. § 1839(3) for the reasons specified in paragraphs 1-2.
4. For Trade Secret 1, the United States will argue that the collection of information in the following documents is a trade secret under 18 U.S.C. § 1839(3) for the reasons specified in paragraphs 1-2.[2]

[1] A "compilation" trade secret can include a compilation of public information or a compilation of proprietary information, including trade secrets, or a mixture of public and proprietary information.

[2] The specification of the information composing Trade Secret 1 in this Bill of Particulars supersedes any past correspondence between the United States and defendants regarding the composition of Trade Secret 1.

a. Trade Secret 2;

b. Trade Secret 3;

c. Trade Secret 4;

d. Trade Secret 5;

e. Trade Secret 6;

f. Trade Secret 7 ;

g. Trade Secret 8;

h. 【DR25nmS】Design rules Periphery_EES_2012000026-013_Rev ( 1).xls;

i. ★★Elpida 25nm process flow_Modify.ppt;

j. ★★Elpida 25nm process flow_peri.ppt;

k. dram_comparison_workshop_100-110_series.pdf;

l. Elpida 25nm process flow.pdf;

m. Template_Tool Mapping_Fab11_Fab16 110sD Tool Risk (F16)-0831 discussion.xlsx;

n. Template_Tool Mapping_Fab11_Fab16 110sD Tool Risk (F16)-0908.xlsx

o. R1 F72 1GC Flow0411 no defect.xls;

p. R1 F72 1GC Flow0411 no defect_1.xls;

q. Rexchip 25nm Flow summary _IMP & RTP.xls;

r. Rexchip 25nm Flow summary 0614 CMP.xls;

s. Rexchip 25nm Flow summary 0614 Diff.xls;

t. Rexchip 25nm Flow summary 0614 Photo.xls;

u. Rexchip 25nm Flow summary 0614 wet.xls;

v. Rexchip 25nm Flow summary 0710 TF.xls; and

w. F32 2014,2015 flow compare-20180824.xlsx.

5. Trade Secret 1 comprises detailed information describing Micron's process flow for creating Dynamic Random Access Memory (DRAM). The combination of process steps, the sequence of process steps, the combination of process recipes/parameters, the combination of process tooling, and the combination of process design rules described in

Trade Secret 1 are each trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2. The combination of that information, considered altogether, is also a trade secret under § 1839(3) for the reasons described in paragraphs 1 and 2.

6. Micron's process flows for DRAM can general be broken into a series of process modules, where each module consists of a sequence of steps directed primarily at a specific aspect of manufacturing DRAM. The process flow information for each such module (including steps, recipes/parameters, and tools) are each independent trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2. Generally, those modules can be described as follows (with some variations between process flows):

   a. Active Area Module: Process sequence that defines the device active areas and creates insulating materials between them.

   b. Well Implant Module: Process sequence where the well and channel implants for electrical devices are formed.

   c. Buried Wordline Module: Process sequence where the buried wordlines are formed across the memory cell arrays.

   d. CMOS Gate-Stack Module: Process sequence where the gate oxides and gate polysilicon layer is formed.

   e. Digtline Module: Process sequence where the bitline contacts are formed and the bitlines and peripheral logic device gates are patterned.

   f. CMOS Transistor Module: Process sequence where the junctions of the various CMOS transistors are formed.

   g. Cell and Local Interconnects Module: Process sequence where the contacts for the call capacitors and the local interconnects in the peripheral regions are formed.

   h. Capacitor Module: Process sequence where the capacitors of the memory cells are formed.

   i. Backend Interconnects Module: Process sequence where the wiring levels to interconnect the various components of the chip together are formed.

7. Accordingly, at least the following subparts of the process-flow information in Trade Secret 1 are independently trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2:

   a. From the file "Rexchip 25nm Flow summary 0614 Diff.xls" ("25nm Summary table" tab):

      i. Rexchip 25 nm process sequence (rows 5-462);

      ii. Active Area Module (rows 5-37);

      iii. Well Implant Module (rows 38-81);

      iv. Buried Wordline Module (rows 82-120);

      v. CMOS Gate-Stack Module (rows 121-145);

      vi. Digitline Module (rows 146-177);

      vii. CMOS Transistor Module (rows 178-235);

      viii. Cell and Local Interconnects Module (rows 236-320);

      ix. Capacitor Module (rows 321-391);

      x. Backend Interconnects Module (rows 392-462);

      xi. Recipe details for the 2G3F (2 Gb DDR 3 DRAM) product in the Rexchip R1 fab (Micron Fab 16) (col. E);

      xii. Recipe details for the 4G3D (4 Gb DDR3 DRAM) product in the Rexchip R1 fab (Micron Fab 16) (col. F);

      xiii. Recipe details for 2G3F (2 Gb DDR3 DRAM) product in the Elpida E300 fab (Micron Fab 15) (col. G); and

      xiv. Recipe details for 4G3D (4 Gb DDR3 DRAM) product in Elpida E300 fab (Micron Fab 15) (col. H).

   b. From the file "Rexchip 25nm Flow summary 0614 Diff.xls" ("25nm 4G3d Flow" tab):

      i. Rexchip 25 nm process sequence for 4G3D product (rows 5 through 486);

      ii. Active Area Module (rows 5-38);

      iii. Well Implant Module (rows 39-80);

iv. Buried Wordline Module (rows 81-122);

v. CMOS Gate-Stack Module (rows 123-151);

vi. Digitline Module (rows 152-187);

vii. CMOS Transistor Module (rows 188-246);

viii. Cell and Local Interconnects Module (rows 247-334);

ix. Capacitor Module (rows 335-411);

x. Backend Interconnects Module (rows 412-486);

xi. Tool in Rexchip R1 fab (Micron Fab 16) (cols. D-E);

xii. Recipe descriptions and parameters in Rexchip R1 fab (Micron Fab 16) (cols. F-G);

xiii. Tool in Elpida E300 fab (Micron Fab 15) (cols. H-I); and

xiv. Recipe information for Elpida E300 fab (Micron Fab 15) (cols. J-K).

c. From the file "Rexchip 25nm Flow summary 0614 Diff.xls" ("25nm 2G3F Flow 含比較" tab):

i. Rexchip 25 nm process sequence for 2G3F product (rows 5 through 481);

ii. Active Area Module (rows 5-38);

iii. Well Implant Module (rows 39-85);

iv. Buried Wordline Module (rows 86-127);

v. CMOS Gate-Stack Module (rows 128-156);

vi. Digitline Module (rows 157-190);

vii. CMOS Transistor Module (rows 191-250);

viii. Cell and Local Interconnects Module (rows 251-334);

ix. Capacitor Module (rows 335-410);

x. Backend Interconnects Module (rows 411-481);

xi. Tools in Rexchip R1 fab (Micron Fab 16) (cols. D-E);

xii. Recipe information for Rexchip R1 fab (Micron Fab 16) (col. F);

xiii. Tools in Elpida E300 fab (Micron Fab 15) (cols. G-H); and

xiv. Recipe information for Elpida E300 fab (Micron Fab 15) (col. I).

d. From the file "Rexchip 25nm Flow summary 0614 Diff.xls" ("2G3F RAWDATA" tab):

i. Combination of process steps (not sorted in sequence) for Micron 2G3F product, that includes measurement and inspection steps not specified in the "25nm 2G3F Flow 含比較" tab (rows 5-750).

e. From the file "F32 2014,2015 flow compare -20150824.xlsx" ("V90B" tab):

i. Micron V90B (4 Gb DDR3 PC DRAM) Fab 16 process sequence dated 8/6/2014 (rows 5-1500, cols. C-G);

ii. Micron V90B (4 Gb DDR3 PC DRAM) Fab 16 process sequence dated 8/24/2015 (rows 5-1500, cols. H-J);

iii. Micron V90B (4 Gb DDR3 PC DRAM) Fab 15 process sequence dated 8/24/2015 (rows 5-1500, cols. V-AB);

iv. Active Area Module (Fab 16, 8/5/2014 ) (cols. C-G, rows 5-127);

v. Active Area Module (Fab 16 8/24/2015 ) (cols. H-J, rows 5-127);

vi. Active Area Module (Fab 15) (cols. V-AB, rows 5-127);

vii. Well Implant Module (Fab 16 8/5/2014) (cols. C-G, rows 128-207);

viii. Well Implant Module (Fab 16 8/24/2015) (cols. H-J, rows 128-207);

ix. Well Implant Module (Fab 15) (cols. V-AB, rows 128-207);

x. Buried Wordline Module (Fab 16 8/5/2014 ) (cols. C-G, rows 208-345);

xi. Buried Wordline Module (Fab 16 8/24/2015) (cols. H-J, rows 208-345);

xii. Buried Wordline Module (Fab 15) (cols. V-AB, rows 208-345);

xiii. CMOS Gate-Stack Module (Fab 16 8/5/2014) (cols. C-G, rows 346-421);

xiv. CMOS Gate-Stack Module (Fab 16 8/24/2015) (cols. H-J, rows 346-421);

xv. CMOS Gate-Stack Module (Fab 15) (cols. V-AB, rows 346-421);

xvi. Digitline Module (cols. C-G, Fab 16 8/5/2014) (rows 422-558);

xvii. Digitline Module (cols. H-J, Fab 16 8/24/2015) (rows 422-558);

xviii. Digitline Module (Fab 15) (cols. V-AB, rows 422-558);

xix. CMOS Transistor Module (Fab 16 8/5/2014) (cols. C-G, rows 559-723);

xx. CMOS Transistor Module (Fab 16 8/24/2015) (cols. H-J, rows 559-703);

xxi. CMOS Transistor Module (Fab 15) (cols. V-AB, rows 559-723);

xxii. Cell and Local Interconnects Module (Fab 16 8/5/2014) (cols. C-G, rows 724-1030);

xxiii. Cell and Local Interconnects Module (Fab 16 8/24/2015) (cols. H-J, rows 704-908);

xxiv. Cell and Local Interconnects Module (Fab 15) (cols. V-AB, rows 724-1030);

xxv. Capacitor Module (Fab 16 8/5/2014) (cols. C-G, rows 1031-1272);

xxvi. Capacitor Module (Fab 16 8/24/2015) (cols. H-J, rows 909-1092);

xxvii. Capacitor Module (Fab 15) (cols. V-AB, rows 1031-1272);

xxviii. Backend Interconnects Module (Fab 16 8/5/2014) (cols. C-G, rows 1273-1498);

xxix. Backend Interconnects Module (Fab 16 8/24/2015) (cols. H-J, rows 1093-1267);

xxx. Backend Interconnects Module (Fab 15) (cols. V-AB, rows 1273-1498);

xxxi. Queue-time information for time-sensitive steps (cols. Q-R); and

xxxii. Process flow recipe information (col. AA).

f. From the file "F32 2014,2015 flow compare -20150824.xlxs" ("2E0F" tab)

i. Micron 2E0F product process sequence for Micron Fab 16 (formerly Rexchip R1 fab) (cols. A-O, rows 5-1224);

ii. Micron 2EOF product process sequence for Micron Fab 15 (formerly Elpida E300 fab) (cols. R-X, rows 5-1238);

iii. Active Area Module (Fab 16) (cols. A-O, rows 5-118);

iv. Active Area Module (Fab 15) (cols. R-X, rows 5-122);

v. Well Implant Module (Fab 16) (cols. A-O, rows 119-205);

vi. Well Implant Module (Fab 15) (cols. R-X, rows 123-202);

vii. Buried Wordline Module (Fab 16) (cols. A-O, rows 206-312);

viii. Buried Wordline Module (Fab 15) (cols. R-X, rows 203-330);

ix. CMOS Gate Stack Module (Fab 16) (cols. A-O, rows 313-380);

x. CMOS Gate Stack Module (Fab 15) (cols. R-X, rows 331-404);

xi. Digitline Module (Fab 16) (cols. A-O, rows 381-483);

xii. Digitline Module (Fab 15) (cols. R-X, rows 405-525);

xiii. CMOS Transistor Module (Fab 16) (cols. A-O, rows 484-637);

xiv. CMOS Transistor Module (Fab 15) (cols. R-X, rows 526-666);

xv. Cell and Local Interconnects Module (Fab 16) (cols. A-O, rows 638-860);

xvi. Cell and Local Interconnects Module (Fab 15) (cols. R-X, rows 667-883);

xvii. Capacitor Module (Fab 16) (cols. A-O, rows 861-1059);

xviii. Capacitor Module (Fab 15) (cols. R-X, rows 884-1064);

xix. Backend Interconnects Module (Fab 16) (cols. A-O, rows 1060-1224); and

xx. Backend Interconnects Module (Fab 15) (cols. R-X, rows 1065-1236).

8. Trade Secret 2 comprises a detailed description of Micron's 90 Series (25 nm) process technology exemplified by the V90B DRAM product. The combination of process steps, the sequence of process steps, and the combination of process recipes/parameters, described in Trade Secret 2 are each trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2. The combination of that information, considered altogether, is also a trade secret under § 1839(3) for the reasons described in paragraphs 1 and 2. Additionally, at least the following subparts of the process-flow information in Trade Secret 1 are independently trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2:

a. Lithographic process technology, describing light source and dry versus wet, used for each patterning level in the 25 nm (4G3D) process flow (p. 17);

b. Hard mask stacks used for various patterning levels for the V90B flow (p.19);

c. Module-by-module list of masking levels used in the Micron 90-series technology p.20);

d. Active Area Module (pp. 22-38);

e. Well Implant Module (pp. 38-49);

f. Buried Wordline Module (pp. 50-67);

g. CMOS Gate-Stack Module (pp. 68-75);

h. Digitline Module (pp. 76-99);

i. CMOS Transistor Module (pp. 100-122);

j. Cell and Local Interconnects Module (pp. 123-173);

k. Capacitor Module (pp. 174-212); and

l. Backend Interconnects Module (rows pp. 213-232).

9. Trade Secret 3 comprises a detailed description of ion-implant conditions used to form electrical devices in Micron's 25 nm DRAM process flow. The combination of all the information in Trade Secret 3 is a trade secret under § 1839(3) for the reasons described in paragraphs 1 and 2. Additionally, at least the following subparts of the information in Trade Secret 3 are independently trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2:

a. Ion implant mask table for transistors and the antifuse used in the Micron 25 nmS Mobile Technology ("08-2_II table1(6ch Ver)" tab, cols. A-AD / rows 1-36);

b. Ion implant mask table for the resistors, diodes, and well contacts used in the Micron 25 nmS Mobile Technology ("09-2_II table1(6ch Ver)" tab, cols. A-AD / rows 1-36);

c. Ion implant mask table for all electrical devices used in the Micron 25 nmS DDR3, DDR4 technology Mobile Technology ("P.3 07 II table" tab, cols. A-AP / rows 1-48);

d. List all of the ion implants for 5 different Micron 25 nm products ("Final" tab, cols. A-AO / rows 1-61);

e. List of the species, dose, energy, and simulated average depth of all the ion-implant steps for the Micron PC V90B product ("Final" tab, cols. D-F);

f. List of the species, dose, and energy of all the ion implant steps for the Micron PC 2E0R product ("Final" tab, cols. H-J);

g. List of the species, does, energy, and simulated average depth of all the ion implant steps for the Micron Mobile 2E0F Product ("Final" tab, cols. K-N);

h. List of the species, dose, and energy of all the ion implant steps for the Micron Mobile V91M product ("Final" tab, cols. O-Q); and

i. List of the species, dose, and energy of all the ion implant steps for the Micron Mobile V9AM product ("Final" tab, cols. R-T);

10. Trade Secret 4 comprises detailed tables of ion-implant parameters used to form electrical devices in Micron's 25 nm DRAM process flows that meet specific, designed-to electrical characteristics for a number of Micron 25 nm products. The combination of all the information in Trade Secret 4 is a trade secret under § 1839(3) for the reasons described in paragraphs 1 and 2. Additionally, at least the following subparts of the information in Trade Secret 4 are independently trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2:

a. Table of ion implant parameters for the Rexchip 25 nm 4G3D (Micron V90B) product ("IMP table-V90B" tab cols. A-O / rows 1-63);

b. Table of ion implant parameters for the Rexchip 25 nm 2E0F product ("IMP table-2E0F" tab cols. A-O / rows 1-63);

c. Table of ion implant parameters for the Rexchip 25 nm Z91B product ("IMP table-Z91B" tab cols. A-O / rows 1-63);

d. Table of ion implant parameters for the Rexchip 25 nm Z90B product ("IMP table-Z90B" tab cols. A-O / rows 1-63);

e. Table of ion implant parameters for the Rexchip 25 nm 2E0R product ("IMP table-2E0R" tab cols. A-O / rows 1-63);

f. Table of ion implant parameters for the Rexchip 25 nm V91M product ("IMP table-V91M" tab cols. A-O / rows 1-63);

g. Table of ion implant parameters for the Rexchip 25 nm V9AM product ("IMP table-V9AM" tab cols. A-O / rows 1-63); and

h. Table of ion implant parameters for the Rexchip 25 nm V99B product ("IMP table-V99B" tab cols. A-O / rows 1-63).

11. Trade Secret 5 comprises a detailed list of Micron's "design rules" for its 25 nm DRAM product. The combination of all the information in Trade Secret 5 is a trade secret under § 1839(3) for the reasons described in paragraphs 1 and 2. Additionally, at least the following subparts of the information in Trade Secret 5 are independently trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2:

a. Active area design rules (Tabs beginning "03"-"07," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

b. Gate design rules (Tabs beginning "08"-"16," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

c. WLIC (M0) design rules (Tabs beginning "17"-"19," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

d. Cell plate design rules (Tab beginning "20," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

e. Periphery Contact design rules (Tabs beginning "21"-"29," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

f. 1st Through Hole design rules (Tabs beginning "30"-"32," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

g. Ion Implantation design rules (Tabs beginning "33"-"38", Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

h. Multi Oxide design rules (Tab beginning "39," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

i. Mark formation design rules (Tab beginning "40," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

j. Plate reverse area design rules (Tab beginning "41," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

k. Block mask design rules (Tabs beginning "42"-"44," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

l. PN isolation design rules (Tabs beginning "45"-"50," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

m. Resistor design rules (Tab beginning "51," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

n. Decoupling capacitance design rules (Tabs beginning "52"-"55," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

o. The definition of final mWL area design rules (Tab beginning "56," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

p. Polyimide design rules (Tab beginning "57," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

q. Antenna design rules (Tabs beginning "58," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri");

r. CMP Dummy design rules (Tabs beginning "59," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri"); and

s. The guideline for image field size of reticle rules (Tabs beginning "60," Tables containing numerical values for "F32-6F MC," "F32-6F Array," and "F32-6F Peri").

12. Trade Secret 6 comprises a detailed description of Micron's 100 Series (20 nm) process technology exemplified by the V00H DRAM product. The combination of process steps, the sequence of process steps, and the combination of process recipes/parameters, described in Trade Secret 6 are each trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2. The combination of that information, considered altogether, is also a trade secret under § 1839(3) for the reasons described in paragraphs 1 and 2. Additionally, at least the following subparts of the process-flow information in

Trade Secret 6 are independently trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2:

a. Active Area Module (pp. 20-39);

b. Well Implant Module (pp. 40-65);

c. Buried Wordline Module (pp. 66-93);

d. CMOS Gate-Stack Module (pp. 94-107);

e. Digitline Module (pp. 108-131);

f. CMOS Transistor Module (pp. 132-173);

g. Cell and Local Interconnects Module (rows pp. 174-218);

h. Capacitor Module (rows pp. 219-261); and

i. Backend Interconnects Module (rows pp. 262-301).

13. Trade Secret 7 comprises a detailed description of Micron's 110 Series (1x nm) process technology exemplified by the Z11A DRAM product dated September 4, 2015. The combination of process steps, the sequence of process steps, and the combination of process recipes/parameters, described in Trade Secret 7 are each trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2. The combination of that information, considered altogether, is also a trade secret under § 1839(3) for the reasons described in paragraphs 1 and 2. Additionally, at least the following subparts of the process-flow information in Trade Secret 7 are independently trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2:

a. Module-by-module list of masking levels used in Micron's 110 Series technology (pp. 20-21);

b. Active Area Module (pp. 35-54);

c. Well Implant Module (pp. 55-66);

d. Buried Wordline Module (pp. 67-85);

e. CMOS Gate-Stack Module (pp. 86-106);

f. Digitline Module (pp. 107-158);

g. An Alternative Digitline Module (pp. 159-178);

h. CMOS Transistor Module (pp. 179-222);

i. Cell and Local Interconnects Module (rows pp. 223-261);

j. Capacitor Module (rows pp. 262-313); and

k. Backend Interconnects Module (rows pp. 314-359).

14. Trade Secret 8 comprises a detailed description of Micron's 110 Series (1x nm) process technology exemplified by the Z11A DRAM product dated November 14, 2014. The combination of process steps, the sequence of process steps, and the combination of process recipes/parameters, described in Trade Secret 8 are each trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2. The combination of that information, considered altogether, is also a trade secret under § 1839(3) for the reasons described in paragraphs 1 and 2. Additionally, at least the following subparts of the process-flow information in Trade Secret 8 are independently trade secrets under § 1839(3) for the reasons described in paragraphs 1 and 2:

a. Module-by-module list of masking levels used in Micron's 110 Series technology (p. 18);

b. Active Area Module (pp. 23-37);

c. Well Implant Module (pp. 38-48);

d. Buried Wordline Module (pp. 49-61);

e. CMOS Gate-Stack Module (pp. 62-78);

f. Digitline Module (w/ cell contacts) (pp. 79-114);

g. CMOS Transistor Module (pp. 115-153);

h. Local Interconnects Module (w/ redistribution layer) (rows pp. 154-180);

i. Capacitor Module (rows pp. 181-225); and

j. Backend Interconnects Module (rows pp. 226-259).

15. The United States intends to rely on evidence at trial that the entirety of information included in Trade Secrets 1-8 meets the definition of "trade secret" in 18 U.S.C. § 1839(3). When a combination of information includes a subset of information that is a trade secret, however, the combination of information is necessarily a trade secret.

16. With respect to Count 7, the United States will prove that Jinhua is liable based on any one of the following, which the United States will prove at trial: (1) receipt, purchase, or possession of an indicted trade secret by an employee, agent, director, or officer of Jinhua in connection with his or her duties and with the intent to benefit Jinhua; (2) aiding and abetting the receipt, purchase, or possession of another of an indicted trade secret by any such employee, agent, director, or officer of Jinhua; or (3) receipt, purchase, or possession of an indicted trade secret by a co-conspirator.

Dated: July 12, 2021

Respectfully Submitted,

STEPHANIE M. HINDS
Acting United States Attorney

/s/ Nicholas O. Hunter
NICHOLAS O. HUNTER
STEVEN MARZEN
Trial Attorneys, National Security Division

LAURA VARTAIN HORN
Assistant United States Attorneys